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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/620,659 | 07/16/2003 | Hiroyuki Takahashi | NEC NEG-298 | 1434 |

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| EXAMINER | |
|---|---|
| TAN, VIBOL | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2819 | |

DATE MAILED: 09/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/620,659 | TAKAHASHI ET AL. | |
| | Examiner | Art Unit | |
| | Vibol Tan | 2819 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *16 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *8,18 and 22* is/are allowed.

6)☒ Claim(s) *1-5,9-12,21,23,24,26 and 27* is/are rejected.

7)☒ Claim(s) *6,7,13-17,19,20 and 25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/16/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-5, 9-12, 23, 24, 26, and 27 are rejected under 35 U.S.C. 102(e) as being anticipated by Rosen (U. S. PAT. 6,549,039).

In claim 1, Rosen teaches all claimed features in Fig. 4, a buffer circuit having an input terminal (B) for receiving an input signal (Clock In) and an output terminal (not marked) for outputting an output signal (/Clock Out), comprising: a first transistor (36) and a second transistor (34) connected in series between a first power supply (Gnd) and a second power supply (Vdd, not marked) having different power supply voltages, each having a control terminal (gate terminal), said first and second transistors being controlled to be on (conducting) and off (not conducting) based on signals respectively fed to said control terminals (terminals of 36 & 34), a connection node (44) between said first and second transistors being connected to said output terminal of said buffer circuit, said control terminal of said first transistor being connected to said input terminal (B) of said buffer circuit; and a control circuit (32) having at least an input terminal (one of the two inputs for 32) for receiving the input signal supplied to said input terminal of

said buffer circuit, and an output terminal for outputting the signal (output from 32) to be supplied to said control terminal of said second transistor, said control circuit performing control so that when the input signal (Clock In) is at a second logic level (logic 1) corresponding to the voltage of said second power supply (Vdd, logic high or 1), said second transistor is turned off (open or not conducting), when the input signal (Clock In) changes from the second logic level (logic 1) to a first logic level (logic 0 or Gnd) corresponding to the voltage of said first power supply, said second transistor is turned on (conducting or closed) to cause a voltage of an output signal of said output terminal of said buffer circuit to change to the voltage of said second power supply (logic 1 or high), thereafter, before the input signal undergoes a transition from the first logic level (logic 0) to the second logic level (logic 1), said second transistor is set to be off, and when the input signal undergoes a transition from the first logic level (logic 0) to the second logic level (logic 1) and said first transistor is switched from off to on, said second transistor is kept off (the functionality of the push-pull circuit).

In claim 2, Rosen further teaches the buffer circuit according to claim 1 wherein, when the input signal (Clock In) fed to said control terminal of said first transistor (36) undergoes a transition from the first logic level (logic 0) to the second logic level (logic 1) and a difference voltage (a difference voltage value between the amplitude of Clock In and Gnd) between a voltage of the signal fed to said control terminal of said first transistor and the voltage of said first power supply exceeds a threshold voltage (the required voltage to turn on a transistor) of said first transistor, said first transistor is turned on, with said second transistor being kept in an off state, to start a transition of

the output signal voltage of said output terminal of said buffer circuit to the voltage of said first power supply (the functionality of the push-pull circuit).

In claim 3, Rosen further teaches the buffer circuit according to claim 1, wherein said control circuit (30, 32) comprises a logic circuit (NAND) generating the signal to be supplied to said control terminal of said second transistor (34) based on a result of a logical operation on the input signal (Clock In) supplied to said input terminal of said buffer circuit and the output signal (/Clock Out or feedback signal) outputted from said output terminal of said buffer circuit, said logic circuit generating a signal at a logic level (logic 0) for turning on said second transistor to supply the generated signal to said control terminal of said second transistor when the input signal supplied to said input terminal of said buffer circuit is at the first logic level ( logic 0) and the output signal outputted from said output terminal of said buffer circuit is at the first logic level (logic 0), and generating a signal at a logic level (logic 1) for turning off said second transistor (34) to supply the generated signal to said control terminal of said second transistor when said second transistor is turned on and the output signal outputted from said output terminal of said buffer circuit gets to the second logic level (see Fig. 5).

In claims 4 and 5, Rosen further teaches the buffer circuit according to claim 1, further comprising a flip-flop circuit (38, 40) having an input terminal connected to said output terminal (44) of said buffer circuit, for storing and holding a logic level of the output signal of said buffer circuit and having an output terminal for outputting a signal which said flip-flop circuit stores and holds, said output terminal of said flip-flop circuit being connected to said output terminal of said buffer circuit; wherein said control circuit

comprises: an inverter (30) having an input terminal for receiving the input signal supplied to said input terminal (B) of said buffer circuit and an output terminal for outputting an inverted signal of the input signal; and a logic circuit (NAND 32) having two input terminals for receiving an inverted signal of the logic level of the output signal of said output terminal of said buffer circuit (as shown in Fig. 4), which is stored and held in said flip-flop circuit, and the output signal from said inverter, and having an output terminal for outputting a signal at the logic level for turning on said second transistor to said control terminal of said second transistor when the signals received at said two input terminals are both at the second logic level (as shown in Fig. 4).

Claim 9, 11, and 12 correspond to detailed circuitry already discussed similar with regard to claims 1-5.

Claims 10, 23, and 24 correspond to detailed circuitry already discussed similar with regard to claims 1-5.

Claims 26 and 27 correspond to detailed circuitry already discussed similar with regard to claims 1-5.

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cheung et al. (U. S. PAT. 6,577,165) in view of Rosen.

In claim 21, Rosen teaches all the claim features of claim 1, where Cheung et al. teaches in Fig. 6, a semiconductor integrated circuit comprising buffer circuit as defined in claim 1, as clock tree.

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to use the buffer clock circuit in the semiconductor for clock tree because it has high gain and it can operate at high speed.

5. Claims 6, 7, 13-17, 19, 20, and 25 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. Claims 8, 18, and 22 appear to comprise allowable subject matters.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vibol Tan whose telephone number is (571) 272-1811. The examiner can normally be reached on Monday-Friday (7:00 AM-4:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike J. Tokar can be reached on (571) 272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vibol Tan

Primary Examiner, AU 2819

VIBOL TAN
PRIMARY EXAMINER